23rd International Symposium on VLSI Design and Test (VDAT-2019)
Indian Institute of Technology Indore, India
July 4 - 6, 2019
www.vdat2019.iiti.ac.in

VLSI Society of India

Call for Papers

Theme of VDAT-2019
Chip to System Design for Artificial Intelligence based Systems

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Women in Engineering Chairs

Sangeeta Nkhate, MANIT, Bhopal, India
Joycee Mekie, IIT Gandhinagar, India
Trapti Jain, IIT Indore, India

Startup Chairs

A. Srivastava, ABVIIITM Gwalior, India
Vimal Bhatia, IIT Indore, India
Himalya Bansal, AutoCiG, IESA, India

Design Contest Chairs

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Ravi Sindal, IET-DAVV, Indore
Kailash Chandra Ray, IIT Patna, India

Website Chairs

Vipul Singh, IIT Indore, India
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Shree Prakash Tiwari, IIT Jodhpur, India

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About VDAT

VDAT began as a small workshop in the year 1998. In 2005, it acquired the status of a Symposium. The purpose of the Symposium is to promote the advancement of all aspects of VLSI. The 23rd International Symposium on VLSI Design and Test (VDAT-2019) is being held in Indian institute of Technology Indore, India. The aim of this symposium is to bring academics, researchers, startups and industrial practitioners together to exchange their ideas in the area of VLSI design, test and system design.

Call for Papers

Researchers, academicians and professionals are invited to submit papers in the following topics (but not limited to)

Devices Modeling and Emerging Devices/Material Technologies

MOS Device Modeling and Simulation; Multi-gate and other Emerging MOS devices. Si-Photonics and Optoelectronics devices; MEMS/NEMS; Organic electronics; 2D and advanced material based electronics; Flash memory devices and other emerging memory technologies like ReRAM, PCM, SSTRAM etc.

VLSI Circuit and System Design

Low power, High-performance and robust design of logic, memory, analog, RF and FPGA based circuits; Clock-generation and distribution circuits including all-digital PLLs and DLLs; ADC's and DAC's; Soft-error and fault-tolerant circuits; Circuit design for reliability effects such as gate oxide integrity, electro-migration, ESD, HCI, NBTI, PBTI etc.; On-chip process, voltage, temperature, and aging sensors and monitoring systems; Hardware accelerators for machine learning (ML) and deep learning algorithms; Hardware implementations of ML algorithms for applications like image/object recognition, computer vision, speech recognition, and natural language processing; ML-based intelligence in IoT under highly constrained design requirements; Secure and intelligent system on chip (SoC) design for automotive, health, defense applications etc.

CAD forVLSI and Hardware Security

Logic and behavioral synthesis; Placement, Routing and Floor planning; CAD tools; Design automation; Hardware attack detection; Threat modeling & defense; Hardware-based security primitive design; Trusted design automation, Tools & Information flow.

Testing and Verification

Design verification, Test, Reliability and Fault tolerance; Formal verification; DFT; Fault modeling; Post-silicon validation; Testing memories and regular logic arrays; Design for manufacturability and yield analysis.

FPGA based Design and Embedded Systems

FPGA based combinational/sequential logic/circuit design, Hardware/Software co-design and verification; Audio, Image and video processing; Reconfigurable systems; Microcontroller, IoT and FPGA based embedded systems design; Embedded software; CAD for embedded systems; Artificial intelligence and ML based systems.

Important Dates

Regular Papers	**Full Paper Submission: ~~March 16,~~ March 31, 2019** **Notification of Acceptance: ~~May 1,~~ May 15, 2019** **Camera Ready Paper: ~~May 1,~~ May 25, 2019**
Tutorials	**Tutorial Proposal Submission: March 18, April 30, 2019** **Tutorial Announcement: ~~April 15,~~ May 31, 2019,**
Student Research	**Full Paper Submission: ~~April 2,~~ May 2, 2019** **Notification of Acceptance: ~~April 25,~~ May 25, 2019** **Camera Ready Paper: ~~April 30,~~ May 30, 2019**
Design Contest	**Submission of Design: ~~April 22,~~ May 7, 2019** **Notification of Acceptance: ~~May 15,~~ May 31, 2019**

Takeaway

Tutorial: Tutorials are invited on the cutting edge research and technology in the area of advanced materials/devices, circuit and systems.

Design Contest: The contest has two divisions. One is to design the analog/digital/RF/mixed signal module using EDA tools and other one is to design and demonstrate the safe and secure intelligent systems using hardware. The forum will provide opportunities to the participants to learn hands on practice for chip to system design (C2SD) and embedded system design using sensors and advanced interface devices.

Fellowship (Travel and Registration): The scheme provides an opportunity to applicants to attend the symposium to enhance technical knowledge. The fellowship covers the travel & registration grant. To avail the fellowship, please keep eye on symposium site.

Submission Link:
https://easychair.org/conferences/?conf=vdat2019

Forums

Student Research Forum: Students, including bachelors, masters and PhDs may participate in this forum through presenting their work for better technical inputs to further improve the quality of work. This forum may also provide an opportunity to the students to establish the network with industry players for job perspective.

Startup Forum: This forum will provide the opportunities to participants to get aware of the various schemes/initiatives offered by the states and central government in chip fabrication, electronics manufacturing clusters, IoT, ML and AI etc. The forum will also provide a platform to the participants to explore the funding opportunities from venture capitalist, by presenting their ideas.

Women in Engineering Forum: The forum will provide the opportunities to the female participants to accelerate their engagement in the area of chip design and autonomous embedded systems.

Submission Instructions

Soft copies of papers should be submitted in **.pdf format** as per the IEEE conference paper format. Papers must not exceed six A4 pages in length and should be uploaded through easy-chair portal. There will be double blind review of the paper. Therefore do not include authors' name in submitted paper. A paper with authors' names will not be considered for review. The paper must include an abstract of about 250 words and maximum of five keywords. The acceptance of the paper is based on the following factors: The purpose of the work; the manner and degree to which it advances the art; specific new results that have been obtained and their significance.

Authors of the accepted papers will be informed by email. Information about necessary revisions will be communicated to the corresponding author through email. The authors will have to incorporate the suggestions and submit the revised camera ready copy of the paper in the given time limit. Along with the paper, authors are required to submit an undertaking form stating that, the paper has not been published previously, it is not under consideration for publication elsewhere, and if accepted will not be published elsewhere in the same form.

It is mandatory for at least one of the authors to register in non-student category for publication of the paper in the proceedings. For the author presenting more than one papers, it is mandatory to register and present each paper separately.

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